Amendment to the Claims:

Applicant selectively amends the claims as follows:

1. (Currently Amended) An apparatus, comprising:

~~a variable speed bus;~~

a first unit coupled to ~~the~~ a variable speed bus, the first unit allocated a first portion of bandwidth on the variable speed bus;

a second unit coupled to the variable speed bus, the second unit allocated a second portion of bandwidth on the variable speed bus; and

~~an arbitration and~~ a ~~bus~~ clock throttling logic ~~control unit~~ to adjust a clock frequency associated with the variable speed bus ~~frequency depending on~~ responsive to a change in at least one of the first unit's utilization of the first portion of bandwidth on the variable speed bus and the second unit's utilization of the second portion of bandwidth on the variable speed bus ~~requirements of the first and second units, the arbitration and bus clock control unit to monitor request rates from the first and second units in order to determine the bandwidth requirements~~.

2. (Original) The apparatus of claim 1, wherein the first unit is a processor unit.

3. (Original) The apparatus of claim 1, wherein the second unit is a video processor unit.

4. (Original) The apparatus of claim 1, wherein the first unit is a hard disk drive controller unit.

5. (Original) The apparatus of claim 1, wherein the second unit is an isochronous data transfer unit.

6. (Canceled).

7. (Currently Amended) The apparatus of claim ~~6~~5, wherein the isochronous data transfer unit is a 1394 controller unit.

8. (Currently Amended) The apparatus of claim ~~6~~5, wherein the isochronous data transfer unit is a USB controller unit.

9. (Canceled).

10. (Currently Amended) A system, comprising:

~~a variable speed bus;~~

a device coupled to ~~the~~ a variable speed bus, the device allocated a portion of bandwidth on the variable speed bus ~~including a bus interface logic unit~~; and

~~an arbitration and bus~~ a clock throttling logic ~~control unit~~ to adjust ~~the~~ a clock frequency associated with ~~of a~~ the variable speed bus ~~depending on~~ responsive to ~~bandwidth requirements of the device coupled to the variable speed bus, the arbitration and bus clock control unit to monitor a request rate from~~ a change in the device's utilization of the allocated portion of bandwidth on ~~coupled to~~ the variable speed bus ~~in order to determine the bandwidth requirements~~.

11. (Currently Amended) The system of claim 10, further comprising:

~~the~~ an arbitration and bus control unit to monitor the device's utilization of the allocated portion of bandwidth and instruct the clock throttling logic to adjust the clock frequency associated with the variable speed bus based on the change in the device's utilization of the allocated portion of bandwidth on the variable speed bus ~~communicate bus frequency information to the bus interface logic unit~~.

12. (Original) The system of claim 10, wherein the device coupled to the variable speed bus is a processor.

13. (Original) The system of claim 10, wherein the device coupled to the variable speed bus is a video processor.

14. (Original) The system of claim 10, wherein the device coupled to the variable speed bus is a hard disk drive controller.

15. (Original) The system of claim 10, wherein the device coupled to the variable speed bus is an isochronous data transfer controller.

16. (Canceled).

17. (Currently Amended) The system of claim ~~16~~15, wherein the isochronous data transfer controller is a 1394 controller.

18. (Currently Amended) The system of claim ~~16~~15, wherein the isochronous data transfer controller is a USB controller.

19-20. (Canceled).

21. (New) The apparatus of claim 1, further comprising:

an arbitration and bus clock throttling unit to monitor the first and the second unit's utilization of respective first and second allocated bandwidths on the variable speed bus and instruct the clock throttling logic to adjust the clock frequency associated with the variable speed bus based on the change in at least one of the first unit's utilization of the first portion of

bandwidth on the variable speed bus and the second unit's utilization of the second portion of bandwidth on the variable speed bus.

22 (New) The apparatus of claim 21, wherein the arbitration and bus clock control unit monitors the first and the second unit's utilization of respective first and second allocated bandwidths on the variable speed bus based on arbitration slots sustained by the first and the second unit over a given time to include a recognition interval.

23. (New) The apparatus of claim 21, wherein the variable speed bus, the first unit, the second unit, the clock throttling logic and the arbitration and clock control unit are located on a single semiconductor die.

24 (New) The apparatus of claim 11, wherein the arbitration and bus clock control unit monitors the device's utilization of the allocated portion of bandwidth based on arbitration slots sustained by the device over a given time to include a recognition interval.